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TITLE: Semiconductor mounting system and semiconductor chip

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INVENTOR-INFORMATION:

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CLAIMS:

What is claimed is:
1. A semiconductor mounting system, comprising a first semiconductor chip in which a first semiconductor integrated circuit is packaged and a second semiconductor chip in which a second semiconductor integrated circuit is packaged,
the first semiconductor chip comprising a plurality of first pins provided on a first surface and a plurality of second pins provided on a second surface,
the second semiconductor chip comprising a plurality of third pins provided on a third surface and a plurality of fourth pins provided on a fourth surface,
the semiconductor mounting system further comprising:
a plurality of first lines for electrically connecting the first pins with the third pins; and
a plurality of second lines for electrically connecting the second pins with the fourth pins, and
a length of the first lines being substantially equal to a length of the second lines.
2. A semiconductor mounting system according to claim 1, wherein the first surface is adjacent to the second surface, and the third surface is adjacent to the fourth surface.
3. A semiconductor mounting system according to claim 1, wherein the first surface opposes the second surface, and the third surface opposes the fourth surface.
4. A semiconductor mounting system according to claim 1, further comprising:
a first substrate on which the first lines are provided; and
a second substrate on which the second lines are provided, wherein
at least one of the first substrate and the second substrate includes a groove for mounting at least one of the first semiconductor chip and the second semiconductor chip.
5. A semiconductor mounting system according to claim 1, wherein:
the first semiconductor chip further comprises a plurality of first pads which are electrically connected to the first pins via a plurality of first wires;
the second semiconductor chip further comprises a plurality of second pads which are electrically connected to the second pins via a plurality of second wires; and

a length of each of the first wires is substantially equal to a length of each of the second wires.
6. A semiconductor mounting system, comprising a semiconductor chip in which a semiconductor integrated circuit is packaged,
the semiconductor chip comprising a plurality of first pins provided on a first surface and a plurality of second pins provided on a second surface,
the semiconductor mounting system further comprising:
a plurality of first lines which are electrically connected to the first pins; and

a plurality of second lines which are electrically connected to the second pins, and
a first plane on which the first lines are provided being substantially perpendicular to a second plane on which the second lines are provided.
7. A semiconductor mounting system according to claim 6, wherein:
a direction in which the first lines extend is substantially parallel to a direction in which the second lines extend; and
the semiconductor chip is substantially perpendicular to at least one of the first plane and the second plane.
8. A semiconductor mounting system, comprising a first semiconductor chip in which a first semiconductor integrated circuit functioning as a master is packaged and a plurality of second semiconductor chips in each of which a second semiconductor integrated circuit functioning as a slave is packaged,
the second semiconductor chips each comprising:
a plurality of first pins provided on a first surface;
a plurality of second pins provided on a second surface which is adjacent to the first surface; and
a synchronization circuit for synchronizing a plurality of signals respectively input to the first pins and for outputting the synchronized signals respectively to the second pins.
9. A semiconductor mounting system according to claim 8, wherein a clock signal is input to one of the first pins, and the synchronization circuit performs a synchronization operation based on the clock signal.
10. A semiconductor mounting system according to claim 8, further comprising a selection circuit for selecting one of: a first path for electrically connecting the first pins respectively with the second pins; and a second path for electrically connecting each of the first pins with the second semiconductor integrated circuit.
11. A semiconductor mounting system according to claim 10, wherein the selection circuit selects one of the first path and the second path based on a selection signal supplied from the first semiconductor chip.
12. A semiconductor mounting system according to claim 10, wherein:
each of the second semiconductor chips further comprises a plurality of terminal resistors respectively corresponding to the first pins; and
each of the terminal resistors is connected to corresponding one of the first pins based on the selection signal.
13. A semiconductor mounting system according to claim 8, wherein the first semiconductor integrated circuit is a memory controller and the second semiconductor integrated circuit is a memory.
14. A semiconductor chip in which a semiconductor integrated circuit is packaged, the chip comprising:
a plurality of first pins provided on a first surface;
a plurality of second pins provided on a second surface which is adjacent to the first surface; and
a synchronization circuit for synchronizing a plurality of signals respectively input to the first pins and for outputting the synchronized signals respectively to the second pins.